REMARKS:

In the outstanding Office Action, claims 1, 5 and 9 were rejected. Claims 2-4 and 6-8 stand cancelled. Claims 1, 5 and 9 are amended for clarification and new claims 10-14 have been added, thus, claims 1, 5 and 9-14 are pending and under consideration. No new matter has been added. The rejections are traversed below.

REJECTION UNDER 35 U.S.C. §102(b):

In the outstanding Office Action, claims 1, 5 and 9 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,519,630 ('630).

'630 discusses an automated design of an LSI according to which existing design data with design procedures thereof are collectively managed in the form of elements so that the elements can be reused.

The present invention discloses a method of processing hierarchically configured design data where design data of a higher rank of hierarchy is set and displayed in a design data of a lower rank of hierarchy so that when the design data of the lower rank is modified after the design data of the higher rank, the wiring data of the higher rank is displayed together with the design data of the lower rank.

The Examiner maintains the comparison of the '630 design system where lower-rank circuit elements are selected upon a selection of higher-rank circuit elements with the present invention. In '630, sets of elements related to design data are classified by function where more specified elements are stored in a lower rank and succeed to all the functions of elements in upper ranks (see, column 6, lines 59-66 of '630). When a design object to be processed has lower-rank design objects, the '630 system retrieves all lower-rank design objects forming the design object so that all the lower-rank design objects are also processed (see, column 17, line 63 through column 18, line 5, column 18, lines 24-27 of '630). For example, as shown in FIG. 23a of '630, when circuit element A is selected, lower-rank circuit elements B, C, D, E and F, which form the circuit element A, are selected (see, column 20, lines 50-64 of '630). This means that the '630 system is limited to modifying/processing lower-rank objects of a design object to be processed and thus, does not teach or suggest referring to higher-rank objects when lower-rank objects are modified subsequent to the upper-rank objects. Further, the '630 method does not teach or suggest a "physical hierarchy" configuration for designing an electric circuit because '630 is limited to retrieving sub-blocks (lower ranks) of a function block (higher rank) during design, which is directed to a logical rank configuration and not a physical rank configuration.

In contrast, the present invention allows reference to design data of an upper rank when layout of a lower rank is modified subsequent to modification of an upper rank design data. As recited in amended independent claims 1 and 5, the method of the present invention includes "obtaining first design data of a lower rank of hierarchy" and "obtaining second design data of a rank of hierarchy higher than the lower rank of hierarchy, after obtaining the first design data... where the hierarchy comprises a physical hierarchy including a plurality of ranks having different physical heights". The first and second design data is then combined such that "when the first design data of the lower rank of hierarchy is modified after the second design data is created, the second design data is displayed together with the first design data of the lower rank of hierarchy" where the hierarchy includes "a physical hierarchy including a plurality of ranks having different physical heights". The '630 system does not teach or suggest "physical hierarchy including ranks having different heights" for designing an electric circuit.

As recited in amended independent claim 9, data of an upper rank is set in the design data of the lower rank and allows "displaying the design data in which the wiring data has been set on a display unit, where when the design data of the lower rank is modified after the wiring data of the upper rank, the wiring data of the upper rank is displayed together with the design data of the lower rank" having hierarchical data having a physical hierarchy including a plurality of ranks having different physical heights. For example, as shown in FIG. 7A and 7B of the present invention, when the layout of the lower rank Ln-1 in the layout structure 110 is modified, the wiring 111 of the upper rank Ln is displayed together with the layout of the lower rank Ln-1. This enables circuit design using a physically lower rank for different purposes, such as considering noise influence or other various evaluations for a relationship between upper and lower rank electrical wiring designs, which may not be directly relevant to a logical circuit design or logical layout but is relevant to physical influence due to vertically different height ranks. This is not taught or suggested by the '630 system which discusses processing of all lower-rank objects of a higher-rank design object upon a selection of the higher-rank design object.

It is respectfully submitted that because the '630 system is limited to retrieving lower-rank objects of a rank structure based on logical configuration of the objects, the present invention is not anticipated by the '630 system. Thus, withdrawal of the outstanding rejection is requested.

NEW CLAIMS:

New claims 10 and 11 have been added to further emphasize a method of processing hierarchically configured design data including "setting and displaying wiring data of a higher rank of the hierarchically configured design data in a design data of a lower rank of the

hierarchically configured design data, where when the design data of the lower rank is modified after the wiring data of the higher rank, the wiring data of the higher rank is displayed together with the design data of the specified rank".

New claims 12-14 are added to emphasize that the design data processing of the present invention includes "retrieving design data of the lower rank" and "retrieving wiring data of an upper rank after retrieving the design data" for "displaying the design data in which the wiring data has been set on a display unit, where the hierarchy comprises a physical hierarchy including a plurality of ranks having different physical heights". This allows flexibility in processing hierarchically structured design data especially in a design situation where design work has been completed on a lower rank design data via processing of a related higher rank data but further processing is necessitated on the lower rank data. Accordingly, the present invention allows wiring data of a higher rank to be referred to while modifying design data of a lower rank.

It is respectfully submitted that the '630 method does not teach or suggest the features of new claims 10-14.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 8/31/4

By: _____

J. Randall Beckers
Registration No. 30,358

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501